UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/904,383	07/12/2001	Chuang-Chieh Lin	67,200-476	1624

7590 07/08/2003

TUNG & ASSOCIATES
Suite 120
838 W. Long Lake Road
Bloomfield Hills, MI 48302

EXAMINER
DEO, DUY VU NGUYEN

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 07/08/2003

4

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/904,383	LIN, CHUANG-CHIEH	
	Examiner	Art Unit	
	DuyVu n Deo	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *16-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *16-20* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Applicant's election of claims 1-15 in Paper No. 3 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are s such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6, 8-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (US 6,197,481) and admitted prior art (pages 1-4 of the specification).

Chang describes a method comprising: exposing a field of a semiconductor having an alignment mark thereon (col. 3, line 15-21, line 40-47); removing the photoresist to producing bare alignment marks ready for the next step (col. 3, line 34-36) (this would read on claimed performing a clear out process around the alignment mark on the field of the semiconductor wafer to reveal the alignment mark). Unlike claimed invention, Chang doesn't describe using a full-image mask. However, he describes using a pattern such as wafer stepper or equivalent (col. 3, line 43-45). Admitted prior art, in page 3, teaches using an image mask to expose the field having the alignment mask. It would have been obvious for one skill in the art at the time of the invention to use any technique known to one skill in the art as long as it can be used to expose the semiconductor, as suggested by Chang that a pattern such as wafer stepper or equivalent, with a reasonable expectation of success.

Referring to claim 11, since the combined method described above using full-image exposure to reveal the alignment mark, which is the same as that of the claimed invention, above method would also produce semiconductor device having greater planar uniformity as compared to using a partial-image exposure on the field to maintain alignment mark.

Referring to claims 2 and 12 admitted prior art teaches (page 3 of the specification) the mask can be a positive photoresist mask.

Referring to claims 3 and 13, Chang shows the field having alignment mark is located at the edge of the semiconductor wafer (figure 1, reference #12).

Referring to claims 5, 6, Chang further describes initially depositing the photoresist on the field of the semiconductor wafer (col. 2, line 11, col. 3, line 9, 10) and removing the photoresist that was exposed (col. 3, line 55-58).

Referring to claim 8, Chang teaches the method further comprising etching the semiconductor wafer (col. 2, line 11-12).

Referring to claim 4, Chang describes the alignment marks are on the near the peripheral of the wafer and admitted prior art (page 2 of the specification) further describes that the alignment marks are on the upper-right and lower-left part of the edge of the semiconductor wafer.

Referring to claims 9 and 10, Chang teaches further removing all of the photoresist (col. 3, line 59-61). This would read on claimed of stripping the photoresist that was unexposed.

4. Claims 7, 14, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang and admitted prior art as applied to claims 6, 11 above, and further in view of Wolf (Silicon Processing for the VLSI Era).

Unlike claimed invention, above prior art doesn't describe developing the photoresist that was exposed. However, Chang describes that the exposed photoresist is removed (col. 3, line 21, 22) and it is the basic technique in the processing of photoresist that the exposed photoresist is removed by a developer (claimed developing the exposed photoresist) as shown here by Wolf (page 407, 429). Therefore, it would have been obvious for one skill in the art to in light of Wolf to develop the exposed photoresist in order to form a photoresist pattern to process the wafer with a reasonable expectation of success.

Drawings

5. Figures 1A, 1B, 2-5 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DuyVu n Deo whose telephone number is 703-305-0515.

DVD
July 2, 2003